

Notice of References Cited	Application/Control No. 10/723,292	Applicant(s)/Patent Under Reexamination BRULS, NIKOLAUS	
	Examiner R. Stephen Dildine	Art Unit 2133	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0053061 A1	05-2002	Kong et al.	714/795
*	B	US-2002/0097821 A1	07-2002	Hebron et al.	375/346
*	C	US-2004/0122883 A1	06-2004	Lee et al.	708/490
*	D	US-2004/0252794 A1	12-2004	Hwang et al.	714/795
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Meier, S.R.; A Viterbi decoder architecture based on parallel processing elements; A Viterbi decoder architecture based on parallel processing elements; Global Telecommunications Conference, 1990, and Exhibition. 'Communications: Connecting the Future', GLOBECOM '90., IEEE; 2-5 Dec. 1990 Pages 1323 - 1327, vol.2
	V	Fettweis, G. et al.; High-speed parallel Viterbi decoding: algorithm and VLSI-architecture; Communications Magazine, IEEE; Volume 29, Issue 5, May 1991; Pages 46 - 55
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.